REMARKS

Claims 1 and 3-18 are pending in the application. Claim 1 has been amended to clarify the subject matter recited therein. No new matter is added by the amendments, which find support throughout the specification and figures. In view of the amendments and the following remarks, favorable reconsideration of this case is respectfully requested.

Applicants note with appreciation that the Examiner acknowledges that claims 4-6 are allowable.

Claims 1, 3, and 7-18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over United States Patent No. 6,507,232 to Matsui (hereinafter Matsui) in view of Japanese Patent Publication No. 2000-208707 to Yusho (hereinafter Yusho). Applicants respectfully traverse.

Claim 1 relates to a semiconductor integrated circuit device that includes, *inter alia*, a terminal and a first capacitance adjusting section which is connected to a wiring between the terminal and a protection resistor in a front stage of an internal circuit. Claim 1 also includes ***a protection circuit which is connected to the wiring between the terminal and the first capacitance adjusting section. The protection circuit of claim 1 protects the internal circuit.***

The Office Action asserts that Matsui discloses a terminal and a first capacitance adjusting section (Office Action; page 3, line 5, to page 4, line 3), but admits that Matsui does not disclose a protection circuit as recited in claim 1. (Office Action; page 4, lines 4-7). The Examiner asserts that the protection circuit connected between the

terminal and the first capacitance adjusting section is shown in Yusho. The Examiner cites figures 4 and 6 of Yusho, and asserts that element 1c of figure 6 discloses a protection circuit and that elements 1d and 1a disclose a terminal and a first capacitance adjusting section, respectively. However, in figure 6 of Yusho, element la is a first stage circuit of an input stage circuit, as described in Yusho. An input stage circuit is different from the capacitance adjusting section of the present invention. In Yusho, the protection circuit and the capacitance adjusting circuit are apparently combined. The capacitance is adjusted by controlling a well potential of a protection element. Therefore, a capacitance range of the capacitance adjustment is limited according to the protection element, and thereby it may be impossible to obtain a desired electric property.

In contrast, in the present invention, the elements for capacitance adjustment are separate and distinct from the elements for input protection. That is, the diffusion capacitance for the capacitance adjustment may be different from the necessary diffusion capacitance for the input protection, and therefore a capacitance range of the capacitance adjustment is not limited by the elements for input protection. Therefore, the present invention enables the achievement of a desirable electric property. Since element 1a disclosed in Yusho does not disclose or suggest a capacitance adjusting section, then element 1c does not disclose a protection circuit connected between a terminal and a first capacitance adjusting section, as recited in claim 1. Therefore, for at least this reason, claim 1 is allowable.

Additionally, the motivation to combine the references results from improper hindsight reasoning. In particular, the Examiner indicates that the motivation to

combine the references is "to enable the protection circuit which is connected to wiring between the terminal and the first capacitance adjusting section of Matsui to be formed and to provide a semiconductor device having a transistor for electrostatic protection ...." (Office Action; page 4, line 13 to page 5, line 3; citing Yusho). Since Matsui does not show a protection circuit, as the Examiner admits at page 4, lines 4-7 of the Office Action, the Examiner uses the result of the combination of the references to justify the combination. Therefore, the present invention provides the only motivation to combine the references, and the combination is therefore improper.

Claims 7-14 ultimately depend from claim 1 and are allowable at least for the same reasons that claim 1 is allowable.

Regarding claim 3, Matsui does not disclose the first and second conductive portions of the first adjusting capacitor, as presented in Remarks section of the previous amendment.

Claim 3 relates to a semiconductor integrated circuit device that includes, *inter alia*, a terminal and a first capacitance adjusting section which is connected to a wiring between said terminal and a protection resistor in a front stage of an internal circuit. In claim 3, a first adjusting capacitor includes a first semiconductive portion which is composed of ***a first well region formed in a substrate with said internal circuit and having a conductive type opposite to that of said substrate***, and a second semiconductive portion which is opposite to said first semiconductive portion and is composed of ***a first diffusion layer region formed in said first well region and having the same conductive type as that of said substrate.***

Matsui does not disclose first and second semiconductive portions as recited in claim 3. The Office Action asserts that Matsui discloses this feature in figures 3 and 4 and at column 7, line 62 to column 8, line 39. (Office Action; page 5, lines 4-17).

However, the capacitance adjusting mechanism of Matsui is apparently a gate of a transistor. On the other hand, the capacitance adjusting section of the present invention, as recited in claim 3, includes a ***diffusion layer***, providing a diffusion capacitance. Matsui discloses that the capacitance is adjusted by disconnecting the capacitor, not by diffusion. Therefore, for at least this reason, claim 3 is allowable.

Additionally, figure 4 of Matsui does not disclose a first semiconductive portion having a first well region formed in a substrate with said internal circuit and having a conductive type opposite to that of said substrate. The section cited in Matsui by the Office Action apparently relates to various transistors of a capacitance adjusting section, and apparently discloses N-type source regions with N-type drain regions (Matsui; col. 8, lines 1-2 and 7-8), and a P-type source region with a P-type drain region (Matsui; col. 8, lines 5-6). However, it does not appear that Matsui discloses or suggests a well region formed in a substrate and having a conductive type ***opposite*** to that of the substrate. Therefore, for at least this additional reason, claim 3 is allowable.

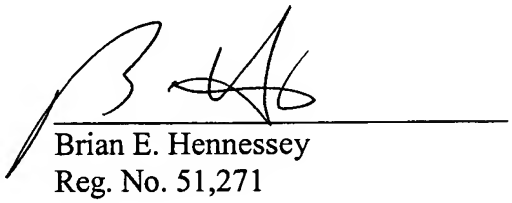
Claims 15-18 ultimately depend from claim 3 and are therefore allowable for at least the same reasons as claim 3 is allowable.

In view of the remarks set forth above, Applicants respectfully submit that the present application is in condition for allowance. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the

Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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